

LISTING OF THE CLAIMS

1. (Previously Presented) An integrated circuit comprising:
 - a processor core;
 - a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions;
 - a bus coupled between said processor core and said configurable peripheral devices, said bus connecting said processor core and said configurable peripheral device without using a sub-processor; and
 - a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.
2. (Previously Presented) The integrated circuit of claim 1 wherein said configurable peripheral device is a universal asynchronous receiver transmitter (UART).
3. (Original) The integrated circuit of claim 2 wherein said UART has a fixed baud rate.
4. (Original) The integrated circuit of claim 1 wherein said processor core, said configurable peripheral device and said bus are implemented on a field programmable gate array.
5. (Previously Presented) The integrated circuit of claim 1 wherein said configurable peripheral device is a flash memory controller.
6. (Previously Presented) A system allowing a user to select peripheral devices in a programmable logic device, comprising:
 - a menu system allowing said user to select one of a plurality of configurable peripheral devices;

a processor core;
a configurable peripheral device comprising a configurable logic block having circuitry capable of implementing a plurality of logic functions;
a bus coupled between said processor core and said configurable peripheral device, said bus connecting said processor core and said configurable peripheral device without using a sub-processor; and
a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.

Claims 7-9. (Cancelled)

10. (Previously Presented) The system of claim 6 wherein said user selectable options comprise at least one of a UART peripheral selector, an Ethernet peripheral selector and a flash memory peripheral selector.

11. (Previously Presented) The system of claim 10 wherein said user selectable options comprise at least one data width size selector responsive to selection of said flash memory peripheral selector.

12. (Previously Presented) The system of claim 10 wherein said user selectable options comprise an error correction selector responsive to selection of said flash memory peripheral selector.

13. (Previously Presented) The system of claim 12 wherein said user selectable options comprise at least one error correction code selector responsive to selection of said error correction selector.

Claims 14-22. (Cancelled)

23. (Previously Presented) The integrated circuit of claim 1 further comprising a configurable input-output block coupled to said configurable logic block, said configurable input-output block coupling signals to and from an external device.

24. (Previously Presented) The integrated circuit of claim 1 wherein said configurable logic block comprises a baud rate generator implemented in configurable logic .

25. (Previously Presented) The integrated circuit of claim 24 wherein said configurable logic block comprises a transmitter-receiver circuit coupled to said baud rate generator and implemented in configurable logic.

26. (Previously Presented) The system of claim 6 wherein said configurable logic block comprises a universal asynchronous receiver transmitter implemented in configurable logic.

27. (Previously Presented) The system of claim 26 wherein said universal asynchronous receiver transmitter comprises a baud rate generator implemented in configurable logic to generate a single baud rate.

28. (Previously Presented) The system of claim 6 further comprising a configurable input-output block coupled to said configurable logic block, said configurable input-output block coupling signals to and from an external device.

29. (Previously Presented) An integrated circuit comprising:
a processor core;
a universal asynchronous receiver transmitter circuit having a baud rate generator implemented in a configurable logic block having circuitry capable of implementing a plurality of logic functions;
a bus coupled between said processor core and said configurable peripheral devices; and

a programmable routing matrix coupled to said configurable logic block, said programmable routing matrix coupling signals to and from said configurable logic block.

30. (Previously Presented) The integrated circuit of claim 29 wherein said processor core comprises a configurable processor core.

31. (Previously Presented) The integrated circuit of claim 29 wherein said baud rate generator has a fixed baud rate.

32. (Previously Presented) The integrated circuit of claim 29 wherein said processor core, said configurable peripheral device and said bus are implemented on a field programmable gate array.